rent through the first double-barrier quantum well is substantially controlled by the voltage in the first conductive base layer.

27. The three-dimensional integrated circuit of claim **26**, wherein the first semiconductor transistor device is p-type and the second semiconductor transistor device is n-type.

28. The three-dimensional integrated circuit of claim **26**, wherein the substrate comprises single crystalline silicon having a top surface parallel to the (100) or (110) crystal plane.

29. The three-dimensional integrated circuit of claim **28**, wherein the single crystalline silicon is placed between the first insulating layer and the first conductive top electrode layer in the first semiconductor transistor device.

30. The three-dimensional integrated circuit of claim **28**, wherein the single crystalline silicon is placed between the first insulating layer and the second conductive bottom electrode layer in the second semiconductor transistor device.

31. The three-dimensional integrated circuit of claim **26**, wherein the first insulating layer comprises single crystalline CaF_2.

32. The three-dimensional integrated circuit of claim **26**, further comprising a second insulating layer positioned between the substrate and the first conductive bottom electrode layer.

33. The three-dimensional integrated circuit of claim **26**, further comprising a contact hole in at least one of the first conductive bottom electrode layer, the first conductive base layer, the first conductive top electrode layer, the second conductive bottom electrode layer, the second conductive base layer, and a second conductive top electrode layer.

34. The three-dimensional integrated circuit of claim **26**, further comprising one or more mesas formed in at least one of the first conductive bottom electrode layer, the first conductive base layer, the first conductive top electrode layer, the second conductive bottom electrode layer, the second conductive base layer, or the second conductive top electrode layer.

35. The semiconductor transistor device of claim **26**, wherein the one or more conductive base regions comprises:

a) a first conductive base region in contact with the first semiconductor barrier region;

b) a semiconductor base barrier region in contact with the first conductive base region; and

c) a second conductive base region in contact with the second semiconductor barrier region.

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